Notice of References Cited	Application/Control No. 10/815,329	Applicant(s)/Patent Under Reexamination DOROJEVETS ET AL.	
	Examiner Dalip K. Singh	Art Unit 2671	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,847,365 B1	01-2005	Miller et al.	345/502
*	B	US-5,226,171	07-1993	Hall et al.	712/9
*	C	US-4,725,973	02-1988	Matsuura et al.	708/520
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	A bit-serial VLSI array processing chip for image processing□□Heaton, R.; Blevins, D.; Davis, E.;□□Solid-State Circuits, IEEE Journal of□□Volume 25, Issue 2, April 1990 Page(s):364 - 368 □□Digital Object Identifier 10.1109/4.52157 □□
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.